Notice of Allowability	Application No.	Applicant(s)	
	10/716,686	VERMEIRE ET AL.	
	Examiner	Art Unit	
	Arleen M. Vazquez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/18/2007*.

2. ☒ The allowed claim(s) is/are *1-47 and 60-67*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Ernest F. Karlsen

ERNEST KARLSEN
PRIMARY EXAMINER

DETAILED ACTION

1. Claims 5, 27-30 and 33-39 are being rejoined and are examined.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Claims 48-59 have been canceled.

4. Rewrite claim 27 as:

27. (Withdrawn-Currently Amended) The IC chip of claim 1, wherein the useful circuit component comprises a gate insulator in a MOS device that is subject to failure due to an ESD event, said prognostic cell comprising a test capacitor having an insulator spacer layer, a coupling circuit that couples a supply voltage and the ESD event to the test capacitor, a stress circuit that increases the supply voltage to the test capacitor and prolongs the ESD event, and a comparison sub-circuit that compares the voltage supported across the test capacitor against a baseline voltage to detect degradation of the insulator spacer layer.

5. Rewrite claim 30 as:

30. (Withdrawn-Currently Amended) The IC chip of claim 1, wherein the useful circuit comprises a MOS device in the IC that is subject to field oxide failure due to radiation effects, said prognostic cell predicts leakage under the field oxide failure

comprising at least one of: a first inverter formed by a current source and a monitor transistor having a gate bias to stress the radiated monitor transistor, said current source being set to an allowed radiation degradation limit for end around leakage between the monitor transistor's source and drain; a second inverter formed by a current source and a monitor transistor having a gate bias to stress the radiated monitor transistor, said current source being set to an allowed radiation degradation limit for device to device leakage in a common well; a third inverter formed by a current source and a monitor transistor having a gate bias to stress the radiated monitor transistor, said current source being set to an allowed radiation degradation limit for device to a neighboring n-well leakage; and a comparator generating the failure indicator when any one of the inverters produces an output that inverts with respect to the baseline.

6. Rewrite claim 33 as:

33. (Withdrawn-Currently Amended) The IC chip of claim 1, wherein the useful circuit component comprises an insulator layer in the IC chip that is subject to failure based on an insulator electric field, said prognostic cell predicting time dependent dielectric breakdown (TDDB) of the insulator layer and comprising a test capacitor with an insulator spacer layer, a coupling circuit that couples a supply voltage from the host IC to the test capacitor, a stress circuit that increases the supply voltage applied to tile test capacitor to create a stressed insulator electric field, and a comparison circuit that compares the voltage supported across the test capacitor against a baseline voltage to detect degradation of the insulator spacer layer.

7. Rewrite claim 36 as:

36. (Withdrawn-Currently Amended) The IC chip of claim 1, wherein the useful circuit comprises a MOS transistor in the IC, said prognostic cell predicting hot carrier degradation of the MOS transistor and comprising test and reference MOS devices with different gate voltages so that the test and reference MOS transistors exhibit, over time, different threshold voltage shifts, and a comparator circuit that generates the failure indicator when the difference in threshold voltages exceeds a preset amount.

Rewrite claim 39 as:

39. (Withdrawn-Currently Amended) The IC chip of claim 1, wherein the useful circuit component comprises interconnect conductors in the IC, said prognostic cell predicting metal migration of the interconnect conductors.

8. Authorization for this examiner's amendment was given in a telephone interview with Mr. Eric Gifford on 07/03/2007.

Reasons for Allowance

9. Claims 1-47 and 60-67 are allowed.

10. The following is an examiner's statement of reasons for allowance:

Claim 1 recites a useful circuit having a component that is subject to possible failure at a time t2 in response to operational stress and a prognostic cell that is statistically designed to fail at a designed trigger time t1 under increased operational stress correlated to the operational stress on the useful circuit by a prognostic distance

of t2-t1 ahead of the useful circuit, in combination with other elements of the claims. Since claims 2-18 and 27-39 depend from claim 1, they are also allowed.

Claim 19 recites said component having a cumulative failure probability C(t) where t2 equals the time at which the failure probability of the useful circuit's component has increased to a fraction f2, and a prognostic cell that is statistically designed to fail with a cumulative trigger probability P(t) where t1 equals the time at which a fraction f1 of the prognostic cells have triggered under increased operational stress correlated to the operational stress on the useful circuit by a prognostic distance equal to t2-t1 ahead of the useful circuit, in combination with other elements of the claims. Since claims 20-26 and 60-62 depend from claim 19, they are also allowed.

Claim 40 recites a useful circuit having a component that is subject to possible failure at a time t2 in response to operational stress and a prognostic cell that is statistically designed to fail at a designed trigger time t1 under increased operational stress correlated to the operational stress on the useful circuit by a prognostic distance of t2-t1 ahead of the useful circuit, in combination with other elements of the claims. Since claims 41-44 depend from claim 40, they are also allowed.

Claim 45 recites a useful circuit having a component that is subject to possible failure at a time t2 in response to operational stress and a oversampled prognostic cell with multiple readout capability that is statistically designed to fail at a designed trigger time t1 under increased operational stress correlated to the operational stress on the useful circuit by a prognostic distance of t2-t1 ahead of the useful circuit, in combination

with other elements of the claims. Since claims 4-47 depend from claim 45, they are also allowed.

Claim 63 recites a useful MOS device that is subject to possible failure due to a threshold voltage shift at a time t2 in response to operational stress; and a prognostic cell that is statistically designed to fail at a designed trigger time t1 by a prognostic distance of t2-tl ahead of the useful MOS device, in combination with other elements of the claims. Since claims 64-67 depend from claim 63, they are also allowed.

These features in combination with other elements of the claims are neither disclosed nor suggested by the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reynick (US 6,873,171) discloses "Integrated circuit early life failure detection by monitoring changes in current signatures".

Moosa et al. (US 5,822,218) discloses "Systems, methods and computer program products for prediction of defect-related failures in integrated circuits".

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arleen M. Vazquez whose telephone number is 571-272-2619. The examiner can normally be reached on Monday to Friday, 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AMV

Ernest J. Karlsen

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